

# **JEDEC STANDARD**

---

**DDR5 SDRAM**

---

**JESD79-5**

**JULY 2020**

---

**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



## NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to [www.jedec.org](http://www.jedec.org) under Standards and Documents for alternative contact information.

Published by  
©JEDEC Solid State Technology Association 2020  
3103 North 10th Street  
Suite 240 South  
Arlington, VA 22201-2108

JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

### **PRICE: Contact JEDEC**

Printed in the U.S.A.  
All rights reserved

## Contents

1	Scope .....	1
1.1	JM7 Verbal Forms and Terms.....	1
1.2	Significance of Light Grey Text in this Document .....	1
2	DDR5 SDRAM Package, Pinout Description and Addressing.....	2
2.1	DDR5 SDRAM Row for X4, X8 .....	2
2.2	DDR5 SDRAM Ball Pitch .....	2
2.3	DDR5 SDRAM Columns for X4, X8 .....	2
2.4	DDR5 SDRAM X4/8 Ballout using MO-210 .....	3
2.5	DDR5 SDRAM X16 Ballout uSing MO-210 .....	4
2.6	Pinout Description .....	5
2.7	DDR5 SDRAM Addressing .....	6
3	Functional Description .....	8
3.1	Simplified State Diagram.....	8
3.2	Basic Functionality .....	9
3.3	Reset and Initialization Procedure .....	9
3.3.1	Power-up Initialization Sequence .....	10
3.3.2	Reset Initialization with Stable Power.....	12
3.3.3	Input Voltage Power-up and Power-Down Sequence .....	13
3.4	Mode Register Definition.....	14
3.4.1	Mode Register Read (MRR) .....	14
3.4.2	Mode Register WRITE (MRW) .....	17
3.4.3	DFE Mode Register Write Update Timing .....	17
3.4.4	Mode Register Truth Tables and Timing Constraints .....	18
3.5	Mode Registers .....	21
3.5.1	Mode Register Assignment and Definition in DDR5 SDRAM .....	21
3.5.2	MR0 (MA[7:0]=00 <sub>H</sub> ) Burst Length and CAS Latency .....	29
3.5.3	MR1 (MA [7:0] = 01 <sub>H</sub> ) - PDA Mode Details .....	30
3.5.4	MR2 (MA [7:0] = 02 <sub>H</sub> ) - Functional Modes MR2 Register Information .....	31
3.5.5	MR3 (MA[7:0]=03 <sub>H</sub> ) - DQS Training.....	32
3.5.6	MR4 (MA[7:0]=04 <sub>H</sub> ) - Refresh Settings .....	33
3.5.7	MR5 (MA[7:0]=05 <sub>H</sub> ) - IO Settings.....	34
3.5.8	MR6 (MA[7:0]=06 <sub>H</sub> ) - Write Recovery Time & tRTP .....	35
3.5.9	MR7 (MA[7:0]=07 <sub>H</sub> ) - RFU .....	35
3.5.10	MR8 (MA[7:0]=08 <sub>H</sub> ) - Preamble / Postamble .....	36
3.5.11	MR9 (MA[7:0]=09 <sub>H</sub> ) - VREF Configuration .....	36
3.5.12	MR10 (MA[7:0]=0A <sub>H</sub> ) - VrefDQ Calibration Value.....	37
3.5.13	MR11 (MA[7:0]=0B <sub>H</sub> ) - Vref CA Calibration Value .....	38
3.5.14	MR12 (MA[7:0]=0C <sub>H</sub> ) - Vref CS Calibration Value .....	39
3.5.15	MR13 (MA [7:0] = 0D <sub>H</sub> ) - tCCD_L .....	40
3.5.16	MR14 (MA[7:0]=0E <sub>H</sub> ) - Transparency ECC Configuration .....	41
3.5.17	MR15 (MA[7:0]=0F <sub>H</sub> ) - Transparency ECC Threshold per Gb of Memory Cells and Automatic ECS in Self Refresh.....	42
3.5.18	MR16 (MA [7:0] = 10 <sub>H</sub> ) - Row Address with Max Errors 1 .....	43
3.5.19	MR17 (MA [7:0] = 11 <sub>H</sub> ) - Row Address with Max Errors 2 .....	43
3.5.20	MR18 (MA [7:0] = 12 <sub>H</sub> ) - Row Address with Max Errors 3 .....	43
3.5.21	MR19 (MA [7:0] = 13 <sub>H</sub> ) - Max Row Error Count .....	44
3.5.22	MR20 (MA [7:0] = 14 <sub>H</sub> ) - Error Count (EC) .....	44
3.5.23	MR21 (MA [7:0] = 15 <sub>H</sub> ) - RFU .....	44
3.5.24	MR22 (MA [7:0] = 16 <sub>H</sub> ) - RFU .....	44
3.5.25	MR23 (MA [7:0] = 17 <sub>H</sub> ) - PPR Settings .....	45
3.5.26	MR24 (MA [7:0] = 18 <sub>H</sub> ) - PPR Guard Key .....	45
3.5.27	MR25 (MA[7:0]=19 <sub>H</sub> ) - Read Training Mode Settings .....	46
3.5.28	MR26 (MA[7:0]=1A <sub>H</sub> ) - Read Pattern Data0 / LFSR0 .....	46
3.5.29	MR27 (MA[7:0]=1B <sub>H</sub> ) - Read Pattern Data1 / LFSR1 .....	47
3.5.30	MR28 (MA[7:0]=1C <sub>H</sub> ) - Read Pattern Invert DQL7:0 (DQ7:0) .....	48